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COMPARISON OF TEMPERATURE DISTRIBUTION IN NANOSIZED TRANSISTORS USING MODERN HEAT TRANSFER THERMAL MODEL

Summary

In this paper two modern electronic structures have been presented. The structures are prototypical Fin Field Effect Transistors. One of them is design in 5 nm technology node while the second one is manufactured by the 12 nm technology node. The temperature distribution in these nanosized structures has been determined and compared between each other. Furthermore, to obtain the temperature distribution in considered electronic structures, the Dual-Phase-Lag model has been applied. This methodology is appropriate for electronic structures produced in nanometric. Apart from that, the comparison to the Fourier-Kirchhoff model has also been prepared. All results have been described and final conclusions have also been presented.

Keywords and phrases: Dual-Phase-Lag model, nanosized structures, FinFETs, temperature distribution, Fourier-Kirchhoff model

1. Introduction

In recent years, the continuous miniaturization of electronic devices is observed. It causes that electronic components have to be changed. In most cases, the structures have reached its scaling limitations and further shrinking, especially below 20 nm, can cause problems [1]. Thus, to follow the continuous technical and technological development and ensure the reliable, fast and low power operation of semiconductors, some changes must be introduced [2] - [3]. The Fin Field-Effect-Transistors (FinFETs) seem to be good candidates to comply with these requirement due to its easier steps of fabrication, better stability and more suitable structure. It contains the double gate as well as triple gate architectures and can be manufactured

on insulator or silicon substrate. However, the technological manufacture of 20 nm structures can lead to occurrence undesirable effects during the devices operation. Thus, the decrease of reliability and operation of equipment in the integrated circuit can be observed. Due to these reasons, it is very important to optimize appearance of mentioned effects and design optimal electronic architecture.

Furthermore, appearance of modern electronic appliances leads to increase of customer requirements. At present, customers want to have small equipment which contains many of different functionalities, such as real-time translation, indication of the way from one to other location, excellent camera and many others. Producers, to meet the expectations of potential buyers, must carefully plan and design electronic structures. Moreover, all phenomena, which may occurred in such small electronic surface, should be taken into account. Additionally, implementation of variety of different application or functionalities in such small devices cause the significant increase of the operation frequency and meaningful generation of the heat density. These mentioned problems can lead to improper operation of the whole equipment and occurrence of the thermal problems. Moreover, they may cause malfunctions or even total damages. Due to these reasons, new solutions of determination of the proper temperature distribution in modern nanosized structures are required. The approach presented in this paper focuses on the Dual-Phase-Lag (DPL) model. This model contains two lags related to the temperature and the heat flux. It was established in 1995 by Tzou [4]. The DPL model can be treated as some modification of the Fourier-Kirchhoff equation. The mathematical description of the DPL model can be expressed by the following equation:

$$\begin{cases} c_v \frac{\partial T(x,y,t)}{\partial t} = -q\,(x,y,t) \\ \\ q\,(x,y,t) + \tau_q \frac{\partial q(x,y,t)}{\partial t} = -k\nabla T\,(x,y,t) - k\tau_T \frac{\partial \nabla T(x,y,t)}{\partial t} \end{cases} \tag{1}$$

where k means the material thermal conductivity, c_v represents the specific-heat capacity, q is the heat flux density, q_{gen} is the heat generation visible inside the structure while T represents the temperature function.

2. Structure Description

The temperature distribution has been determined in two similar structures, 5 and 12 nm FinFETs. The schematic three-dimensional structure of the FinFET is presented in Figure 1 [5], [6].

Taking into account that temperature is generated inside the structure of FinFET, the part of demonstrated structure is considered only. This part consist of, inter alia, dielectrics, gates and channels. The cross-sectional views of investigated parts of 5 and 12 nm FinFETs are shown in Figure 2a and Figure 2b, respectively. The cross-

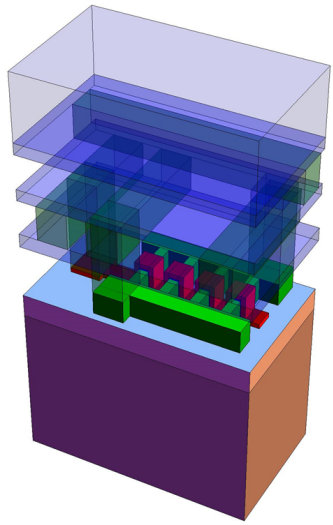


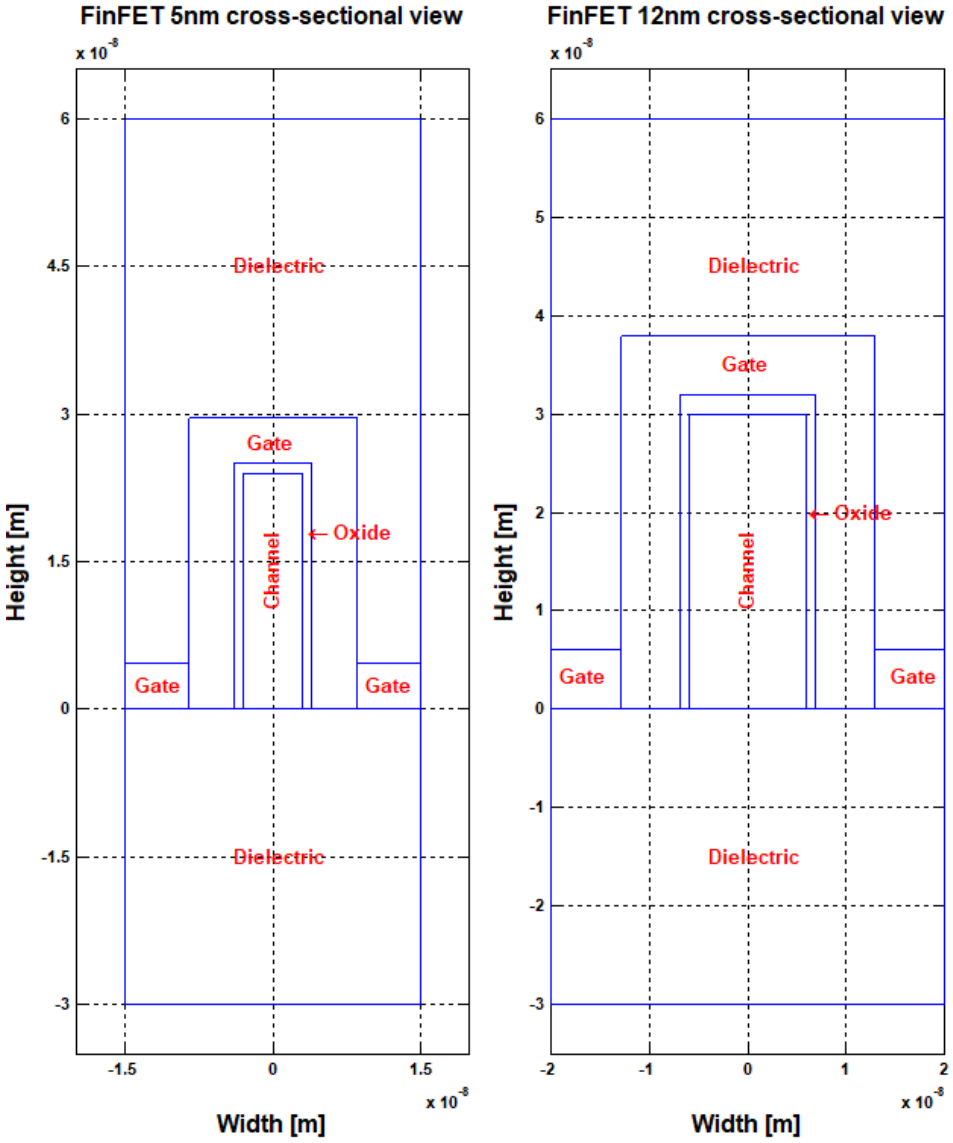
Fig. 1: Schematic 3D view of FinFET

sectional views have been made along the channels lenght in the middle part of the structure. The explanations of all symbols visible in the figures and corresponding values are presented in Table 1 [7].

Symbol name	Symbol	5 nm FinFET [nm]		12 nm FinFET [nm]	
		Width	Height	Width	Height
Channel	Ch	6	24	12	30
Gate	G	4.6 (cross-section)		6 (cross-section)	
Dielectric 1	D1	1 (cross-section)		1 (cross-section)	
Dieletric 2	D2	30	90	40	90

As it is clearly visible, the difference between different structure is observed in their size and dimensions. 12 nm FinFEt has bigger values of their elements than 5 nm structure. The heights of investigated FinFETs structures are equal to 90 nm while their widths are a little different. In the case of 5 nm FinFET its width is equal to 30 nm. For 12 nm FinFET this dimension is equal to 40 nm. The similar values in both cases is also observed in the case of dielectric (D1), which is located between the gate (G) and the channel (Ch). It is made of aluminum oxide and its cross-sectional width is equal to 1 nm. Totally different values of size are visible in channels and gates. The channel is made of the silicon and in the case of 5 nm FinFET its width is equal to 6 nm while in the case of 12 nm FinFET it is equal to 12 nm. Moreover, the height of the channel is different and it is equal to 24 and 30 nm for 5 nm FinFET and 12 nm FinFETs, respectively. The gate is encompassed by the dielectric and it

is located over the substrate. The cross-sectional width of the gate in the case of 5 nm FinFET is 4.6 nm while in 12 nm FinFET structure its width is 6 nm.



(a) Cross-sectional view of 5 nm FinFET (b) Cross-sectional view of 12 nm FinFET

3. Simulation

Presented results of simulations have been carried out in the Matlab environment. As it was mentioned earlier, the temperature distribution determination has been obtained using the Dual-Phase-Lag model. Moreover, the comparison with commonly used Fourier-Kirchhoff approach has also been included. Furthermore, to prepared the numerical implementation of mentioned heat transfer model, the Finite Element Method has been applied. Next, the obtained values of the temperature rises have been normalized. The normalization procedure is expressed by the ratio of obtained value of the temperature in certain discretization node and the value of the maximal temperature received during the simulation process. Its mathematical description can be expressed by the following formula:

$$T_{normalized} = \frac{T}{T_{maximal}} \tag{2}$$

It is also worth mentioning that value of the maximal temperature during the simulation process mean the maximal observed temperature in the case of both analyzed FinFETs structures. The normalization is usually applied to make the analyses and comparisons easier to interpret. All received normalized temperature distributions are presented in Figure 3 - 10 for 5 nm and 12 nm FinFETs, respectively.

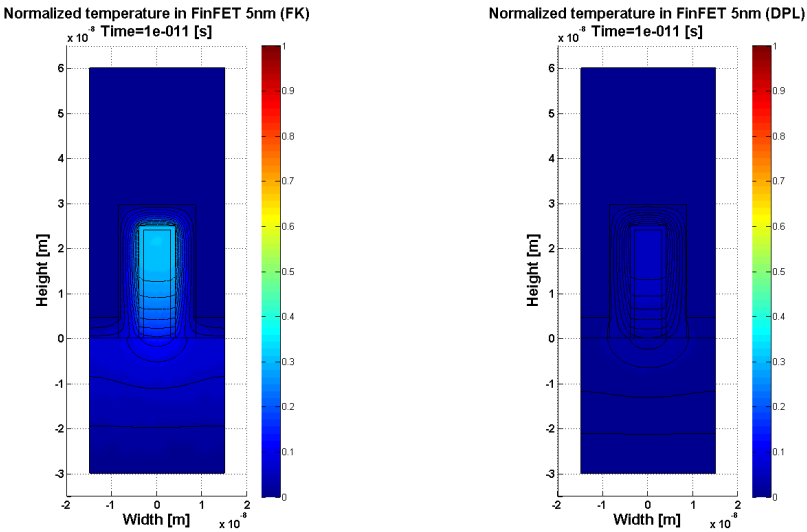


Fig. 3: The temperature distribution in 5 nm FinFET using FK and DPL models at the beginning of the simulation process

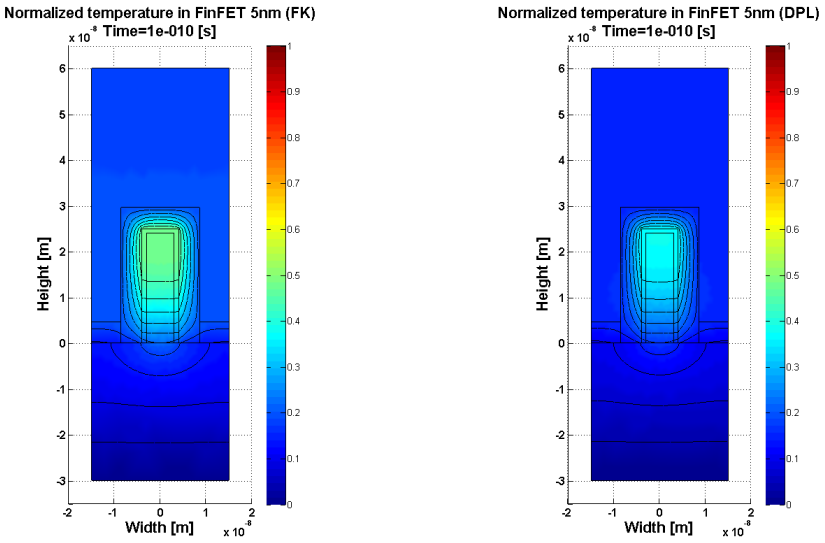


Fig. 4: The temperature distribution in 5 nm FinFET using FK and DPL models - transient analysis (part I)

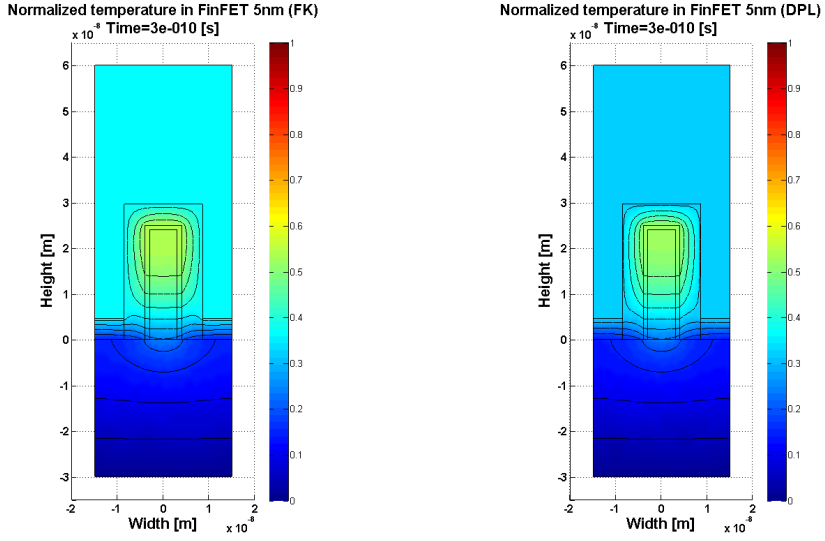


Fig. 5: The temperature distribution in 5 nm FinFET using FK and DPL models - transient analysis (part II)

Figures 3 - 6 present the determination of the temperature distribution in 5 nm FinFET using both FK model and DPL model. As it is visible, demonstrated results are prepared for different time instants of the simulation process. Moreover, it can be observed that in initial part of simulation, presented in Figure 3 and Figure 4, the temperature differences between FK and DPL approaches are clearly visible. The FK model generates higher values of the temperature since the beginning of the simulationtime while the DPL methodology determines significantly lower values of the temperature. In further part of the simulation process, these differences are less visible, what can be seen in Figure 5. While higher values of the temperature are received in the case of FK approach, the obtained results in DPL model are smaller. Moreover, the steady-state temperature is faster obtained for FK than DPL one. However, in the steady state the temperature distributions are the same for both investigated models, what is presented in Figure 6. This is, of course, the proper results from the physical point of view.

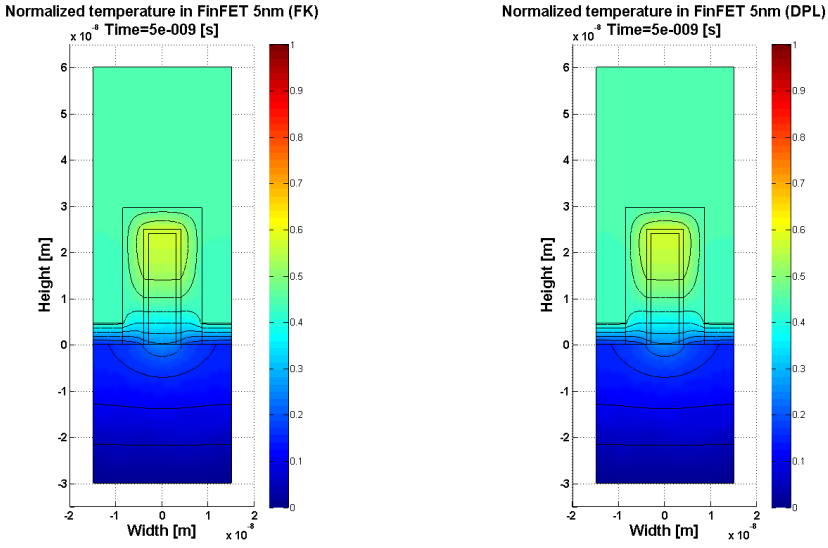


Fig. 6: The steady-state temperature distribution in 5 nm FinFET using FK and DPL models

On the other hand, the temperature distributions in 12 nm FinFET structure for both FK and DPL models are presented in Figures 7 - 10. Results are demonstrated for different time instants. Similarly to the previously analyzed structure, the differences between FK model and the DPL one are clearly visible. The temperature values are meaningfully higher in the case on FK model. Moreover, the steady-state is also quickly obtained for the FK model, however the steady state temperature distributions are exactly the same for both analyzed thermal models.

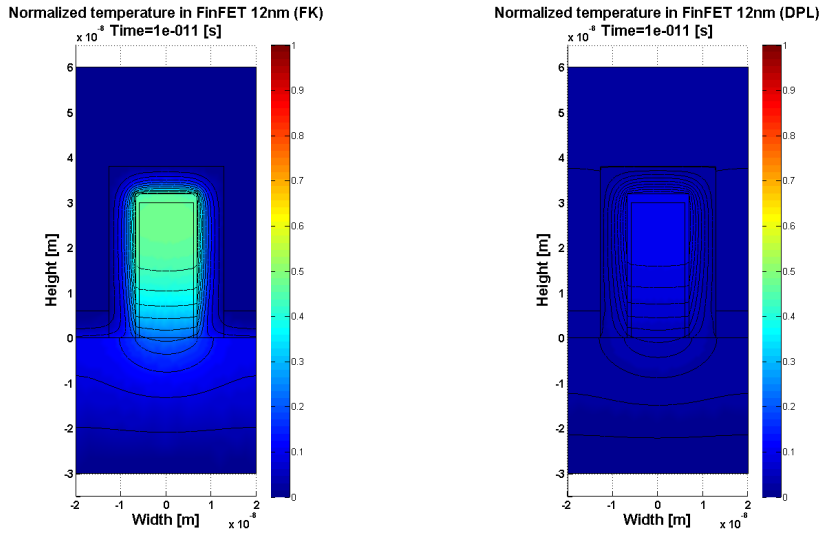


Fig. 7: The temperature distribution in 12 nm FinFET using FK and DPL models at the beginning of the simulation process

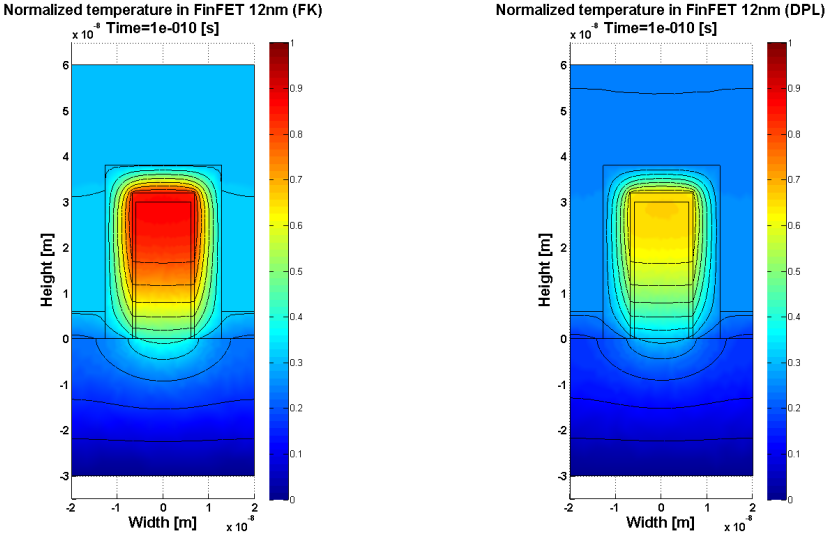


Fig. 8: The temperature distribution in125 nm FinFET using FK and DPL models - transient analysis (part I)

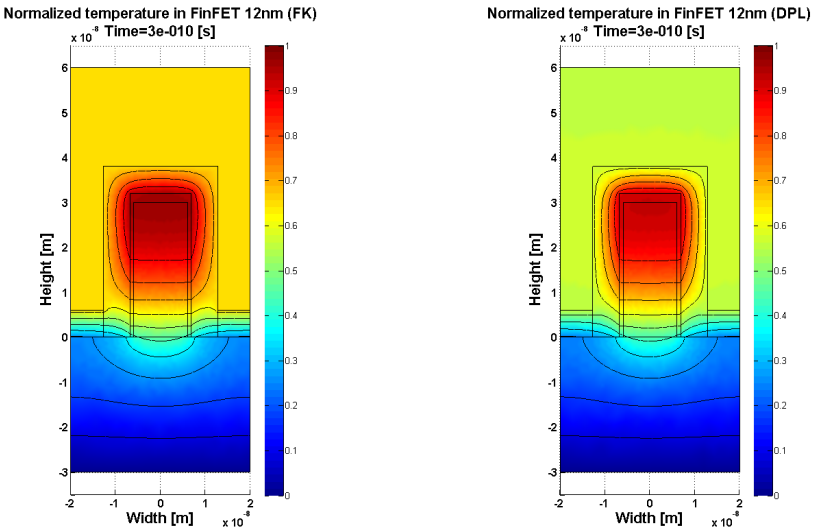


Fig. 9: The temperature distribution in 12 nm FinFET using FK and DPL models - transient analysis (part II)

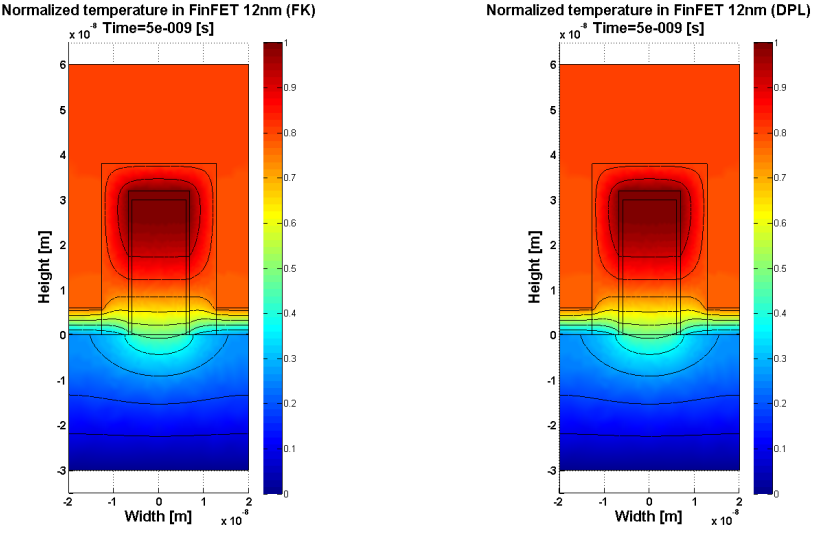


Fig. 10: The steady state temperature distribution in 12 nm FinFET using FK and DPL models

As it is visible, significant differences are observed between temperature distributions obtained for 5 nm and 12 nm FinFET structures. First of all, the cross-sectional area is bigger in the case of 12 nm structure. Moreover, the temperature values for both FK and DPL models are higher in the case of 12 nm FinFET taking into consideration the same current and voltage levels. Considering results presented in Figures 3 - 10 the difference is clearly visible. While in 5 nm structure the obtained temperature values are relatively small, in the case of 12 nm FinFET the steady-state temperature rises are significantly higher.

Apart from that, the average normalized temperature rises obtained in the case of 5 and 12 nm FinFETs have been analyzed and presented presented in Figure 11. The results obtained in the case of 5 nm structure are marked by the solid lines while for 12 nm FinFET are marked by dashed lines. The temperature rises determined by FK model are represented by red color. The green lines present results obtained in the case of DPL model. As it is visible, average normalized temperature rises in the FinFET channels are higher in the case of 12 nm FinFET while the values of the temperature rises visible in 5 nm structure are significantly smaller. Moreover, as it was mentioned earlier, the FK model in both cases produces higher values of the temperature rises in the initial part of the thermal analysis. Moreover, the DPL model results are lagged in relation to the FK model. When in both models the steady state is reached, the determined temperature curves coincide.

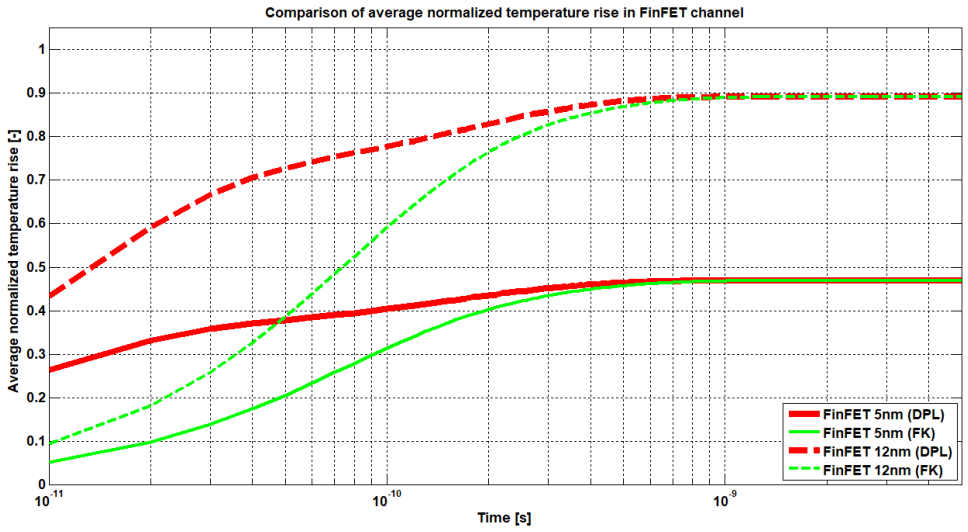


Fig. 11: Comparison of average normalized temperature rises obtained for 5 and 12 nm FinFETs

On the other hand, the maximal normalized temperature rises in the case of FK and DPL models are presented in Figure 12.

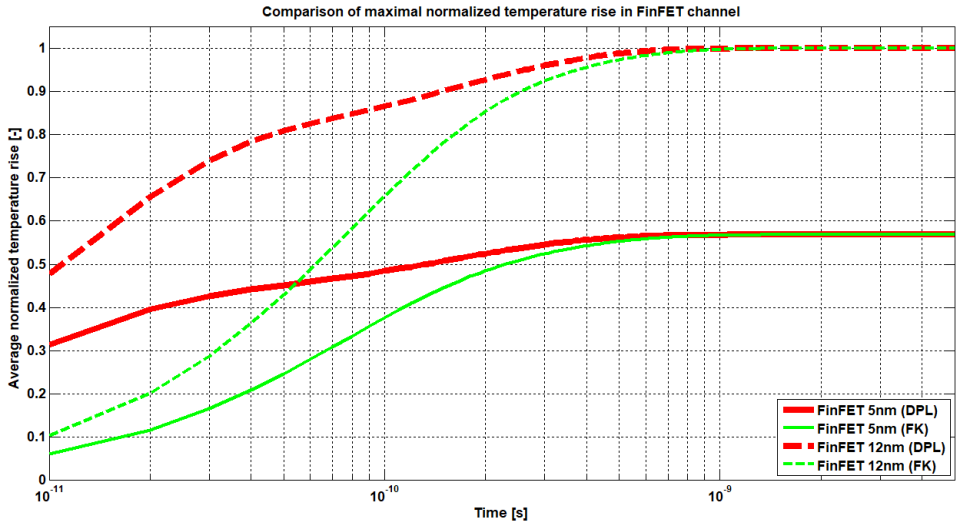


Fig. 12: Comparison of maximal normalized temperature rises obtained for 5 and 12 nm FinFETs

As it is visible, the character of changes of the temperature rises is also very similar to the previous analyses. In demonstrated consideration, the temperature rises are slightly higher than these ones presented in Figure 11. The steady state temperature rises in the case of 12 nm FinFET tend to the 1 while the steady state temperatures for 5 nm are approximately equal to 0.58. Thus, 12 nm FinFET produces almost two times higher temperatures than 5 nm structure.

4. Conclusions

In this paper, the comparison of the temperature distribution in two nanosized FinFET structures has been presented. The temperature distribution has been determined using the Dual-Phase-Lag model. Obtained results have been compared with those ones received using the classical Fourier-Kirchhoff model.

As it occurred, the temperature values produced by Fourier-Kirchhoff approach are significantly higher than those ones obtained by the application of the Dual-Phase-Lag model. Moreover, the steady state is reached faster in the case of Fourier-Kirchhoff model than the Dual-Phase-Lag one. Furthermore, taking into consideration the same current and voltage levels, the generated temperature rises are significantly higher in the case of 12 nm FinFET structure than in the case of 5 nm

FinFET one. It can be explained by bigger area of the heat generation in the case of 12 nm FinFETs than in the case of 5 nm FinFET. It means that structures developed in smaller technology node can achieve higher operation frequencies. However, in order to proper design of the power management profiles, the modern Dual-Phase-Lag model should be used instead of the classical Fourier-Kirchhoff one.

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PORÓWNANIE ROZKŁADÓW TEMPERATURY W NANOTRANZYSTORACH PRZY UŻYCIU NOWOCZESNEGO MODELU TERMICZNEGO

S t r e s z c z e n i e

W pracy przedstawiono porównanie rozkładów temperatur w dwóch nanometrycznych strukturach elektronicznych. Pierwszą z nich jest prototypowy tranzystor FinFET zaprojektowany w procesie technologicznym 5nm. Drugą rozważaną strukturą jest tranzystor FinFET wykonany w procesie technologicznym 12 nm. W celu wyznaczenia rozkładu temperatury w analizowanych strukturach wykorzystano nowoczesny model termiczny Dual-Phase-Lag. Dodatkowo, wszystkie otrzymane wyniki porównane zostały z temperaturami uzyskanymi przy użyciu klasycznego modelu Fouriera-Kirchhoffa. Zaprezentowane wyniki zostay szczegółowo opisane w artykule. Przedstawiono ponadto najważniejsze wnioski w formie krótkiego podsumowania.

Słowa kluczowe: model Dual-Phase-Lag, struktury nanometryczne, tranzystor FinFET, rozkład temperatury, model Fouriera-Kirchhoffa